Data Sheet FN3072.7

CMOS Voltage Converters

The Intersil ICL7660 and ICL7660A are monolithic CMOS power supply circuits which offer unique performance advantages over previously available devices. The ICL7660 performs supply voltage conversions from positive to negative for an input range of +1.5V to +10.0V resulting in complementary output voltages of -1.5V to -10.0V and the ICL7660A does the same conversions with an input range of +1.5V to +12.0V resulting in complementary output voltages of -1.5V to -12.0V. Only 2 noncritical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660 and ICL7660A can also be connected to function as voltage doublers and will generate output voltages up to +18.6V with a +10V input.

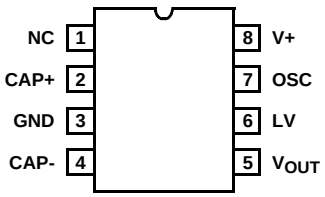
Contained on the chip are a series DC supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-Channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0V. This frequency can be lowered by the addition of an external capacitor to the “OSC” terminal, or the oscillator may be overdriven by an external clock.

The “LV” terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5V to +10.0V for the ICL7660 and +3.5V to +12.0V for the ICL7660A), the LV pin is left floating to prevent device latchup.

Pinouts

ICL7660, ICL7660A
(8 LD PDIP, SOIC)
TOP VIEW



Features

- Simple Conversion of +5V Logic Supply to ±5V Supplies
- Simple Voltage Multiplication (V_{OUT} = (-) nV_{IN})
- Typical Open Circuit Voltage Conversion Efficiency 99.9%
- Typical Power Efficiency 98%
- Wide Operating Voltage Range
  - ICL7660 . . . . . 1.5V to 10.0V
  - ICL7660A . . . . . 1.5V to 12.0V
- ICL7660A 100% Tested at 3V
- Easy to Use - Requires Only 2 External Non-Critical Passive Components
- No External Diode Over Full Temp. and Voltage Range
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- On Board Negative Supply for Dynamic RAMs
- Localized μProcessor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

Ordering Information

PART NUMBER		TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ICL7660CBA*	7660CBA	0 to 70	8 Ld SOIC (N)	M8.15
ICL7660CBAZ* (See Note)	7660CBAZ	0 to 70	8 Ld SOIC (N) (Pb-free)	M8.15
ICL7660CBAZA* (See Note)	7660CBAZ	0 to 70	8 Ld SOIC (N) (Pb-free)	M8.15
ICL7660CPA	7660CPA	0 to 70	8 Ld PDIP	E8.3
ICL7660CPAZ (See Note)	7660CPAZ	0 to 70	8 Ld PDIP** (Pb-free)	E8.3
ICL7660ACBA*	7660ACBA	0 to 70	8 Ld SOIC (N)	M8.15
ICL7660ACBAZA* (See Note)	7660ACBAZ	0 to 70	8 Ld SOIC (N) (Pb-free)	M8.15
ICL7660ACPA	7660ACPA	0 to 70	8 Ld PDIP	E8.3
ICL7660ACPAZ (See Note)	7660ACPAZ	0 to 70	8 Ld PDIP** (Pb-free)	E8.3
ICL7660AIBA*	7660AIBA	-40 to 85	8 Ld SOIC (N)	M8.15
ICL7660AIBAZA* (See Note)	7660AIBAZ	-40 to 85	8 Ld SOIC (N) (Pb-free)	M8.15

*Add “-T” suffix to part number for tape and reel packaging.

**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply Voltage
- ICL7660 . . . . . +10.5V
- ICL7660A . . . . . +13.0V

LV and OSC Input Voltage . . . . . -0.3V to (V+ +0.3V) for V+ < 5.5V
(Note 2) . . . . . (V+ -5.5V) to (V+ +0.3V) for V+ > 5.5V
Current into LV (Note 2) . . . . . 20μA for V+ > 3.5V
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) . . . . . Continuous

Operating Conditions

Temperature Range
- ICL7660C, ICL7660AC. . . . . 0°C to 70°C
- ICL7660AI . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package*	110	N/A
SOIC Package	160	N/A

Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

ICL7660 and ICL7660A, V+ = 5V, T_A = 25°C, C_{OSC} = 0, Test Circuit Figure 11 Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	ICL7660			ICL7660A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	I+	$R_L = \infty$	-	170	500	-	80	165	μA
Supply Voltage Range - Lo	V_L+	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to GND	1.5	-	3.5	1.5	-	3.5	V
Supply Voltage Range - Hi	V_H+	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to Open	3.0	-	10.0	3	-	12	V
Output Source Resistance	R_{OUT}	I_{OUT} = 20mA, T_A = 25°C	-	55	100	-	60	100	Ω
		I_{OUT} = 20mA, 0°C ≤ T_A ≤ 70°C	-	-	120	-	-	120	Ω
		I_{OUT} = 20mA, -55°C ≤ T_A ≤ 125°C	-	-	150	-	-	-	Ω
		I_{OUT} = 20mA, -40°C ≤ T_A ≤ 85°C	-	-	-	-	-	120	Ω
		V^+ = 2V, I_{OUT} = 3mA, LV to GND 0°C ≤ T_A ≤ 70°C	-	-	300	-	-	300	Ω
		V+ = 2V, I_{OUT} = 3mA, LV to GND, -55°C ≤ T_A ≤ 125°C	-	-	400	-	-	-	Ω
Oscillator Frequency	f_{OSC}		-	10	-	-	10	-	kHz
Power Efficiency	P_{EF}	R_L = 5kΩ	95	98	-	96	98	-	%
Voltage Conversion Efficiency	$V_{OUT\ EF}$	$R_L = \infty$	97	99.9	-	99	99.9	-	%
Oscillator Impedance	Z_{OSC}	V+ = 2V	-	1.0	-	-	1	-	MΩ
		V = 5V	-	100	-	-	-	-	kΩ
ICL7660A, V+ = 3V, T_A = 25°C, OSC = Free running, Test Circuit Figure 11, Unless Otherwise Specified									
Supply Current (Note 3)	I+	V+ = 3V, $R_L = \infty$, 25°C	-	-	-	-	26	100	μA
		0°C < T_A < 70°C	-	-	-	-	-	125	μA
		-40°C < T_A < 85°C	-	-	-	-	-	125	μA
Output Source Resistance	R_{OUT}	V+ = 3V, I_{OUT} = 10mA	-	-	-	-	97	150	Ω
		0°C < T_A < 70°C	-	-	-	-	-	200	Ω
		-40°C < T_A < 85°C	-	-	-	-	-	200	Ω
Oscillator Frequency (Note 3)	f_{OSC}	V+ = 3V (same as 5V conditions)	-	-	-	5.0	8	-	kHz
		0°C < T_A < 70°C	-	-	-	3.0	-	-	kHz
		-40°C < T_A < 85°C	-	-	-	3.0	-	-	kHz

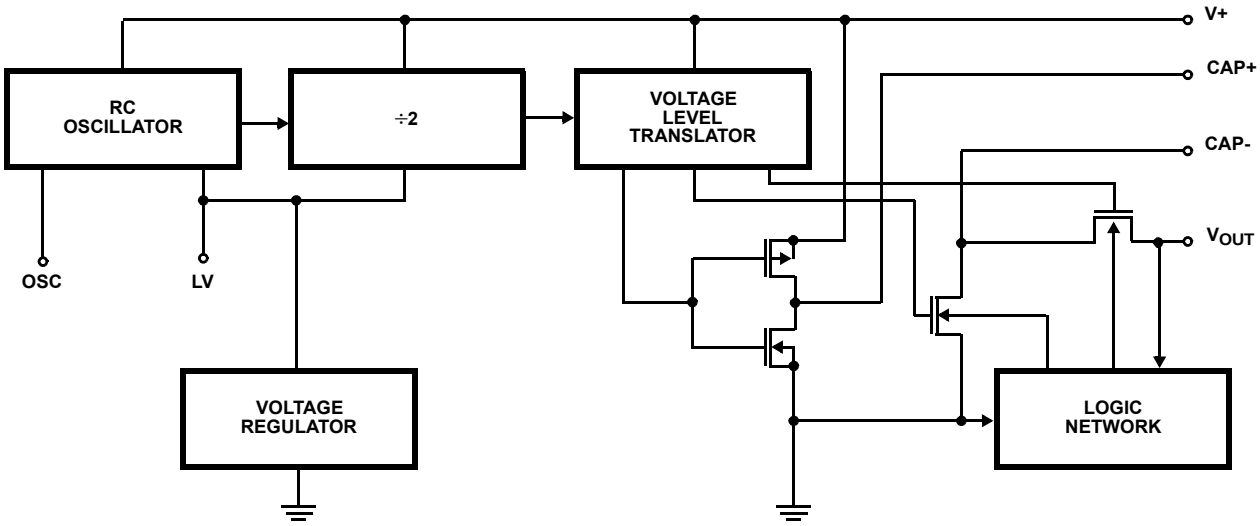
Electrical Specifications ICL7660 and ICL7660A, V+ = 5V, T_A = 25°C, C_{OSC} = 0, Test Circuit Figure 11 Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	ICL7660			ICL7660A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Conversion Efficiency	$V_{OUT}EFF$	V+ = 3V, $R_L = \infty$	-	-	-	99	-	-	%
		$T_{MIN} < T_A < T_{MAX}$	-	-	-	99	-	-	%
Power Efficiency	P_{EFF}	V+ = 3V, R_L = 5kΩ	-	-	-	96	-	-	%
		$T_{MIN} < T_A < T_{MAX}$	-	-	-	95	-	-	%

NOTES:

2. Connecting any input terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to “power up” of the ICL7660, ICL7660A.
3. Derate linearly above 50°C by 5.5mW/°C.
4. In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of 5pF.
5. The Intersil ICL7660A can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.

Functional Block Diagram



Typical Performance Curves (Test Circuit of Figure 11)

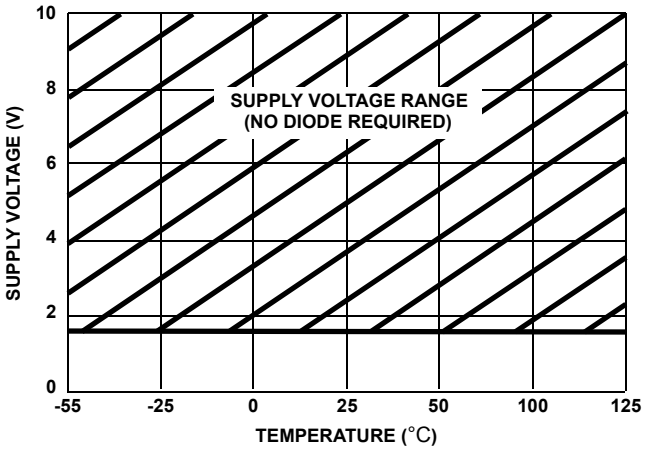


FIGURE 1. OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE

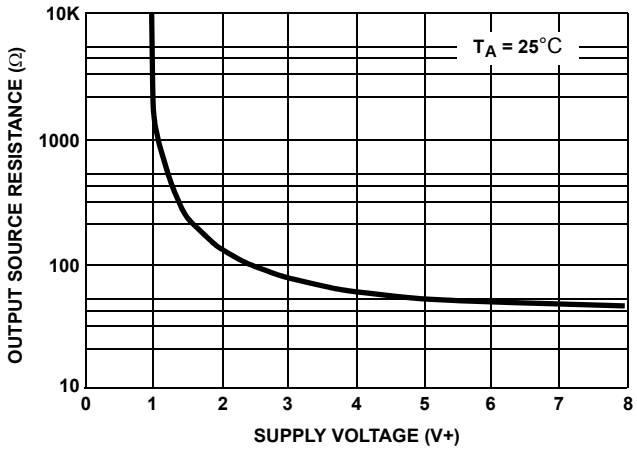
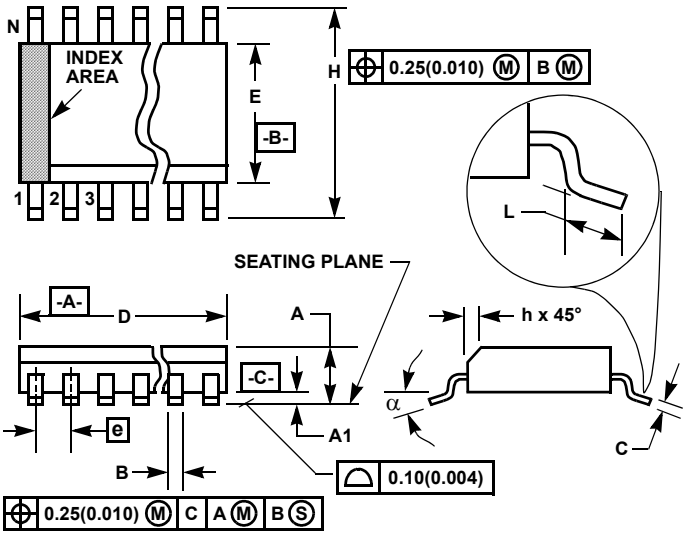


FIGURE 2. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE

Small Outline Plastic Packages (SOIC)



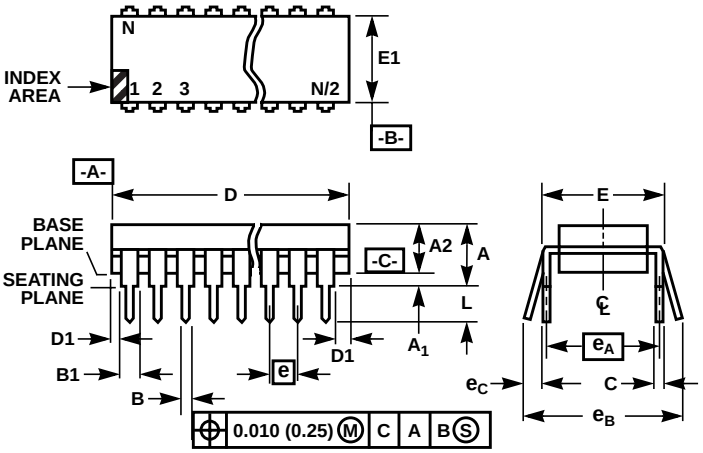
NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9